

Innovations in Wafer Level Technology

A proven leader in Wafer Level Packaging technology



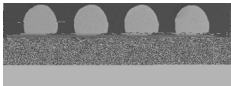
eWLCSP™ and FI-ECP

We offer two types of Fan-in WLP with protective sidewall coating – encapsulated Wafer Level Chip Scale Packaging (eWLCSP) and Fan-in Encapsulated Chip Package (FI-ECP).

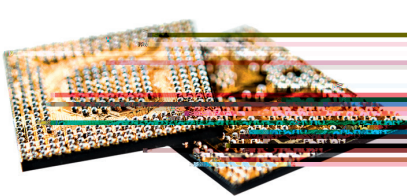
With eWLCSP, the formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the same high volume reconstitution and wafer level molding process that is used for our Fan-out embedded Wafer Level Ball Grid Array (eWLB) technology.

FI-ECP has a similar package structure, but follows a different manufacturing flow based on plasma dicing and the lamination process.

If your application requires body sizes below 3x3mm and very thin silicon die, FI-ECP will provide a robust solution to meet your needs. For body sizes above 3x3mm and standard die thicknesses, eWLCSP will provide the best solution.

eWLCSP	FI-ECP
Large body size (>3x3mm)	Smaller body size (<3x3mm)
Standard Si die thickness (350 - 400 μm)	Very thin Si die (100 -150 μm)
Reconstitution and wafer level molding process similar to Fan-out Wafer Level Packaging	Plasma dicing and lamination process
	

Fan-out WLP: High Performance, High Density Solution



Fan-out Wafer Level Packaging (FOWLP) is an advanced packaging technology platform that provides a high density interconnection, superior electrical performance

and the ability to integrate multiple heterogeneous dies in a cost effective, low-profile semiconductor package.

The fan-out structure enables the interconnects to be routed to the outside of the die, thus reducing the amount of silicon real estate needed to accommodate very high input/output (I/O) densities.

By eliminating the discrete chip-to-package interconnect that typically requires a flip chip bump or wirebond, FOWLP

delivers measurable advantages in cost, reliability and performance.

FOWLP devices are manufactured with a chip-first or a chip-

eWLB	FO-ECP
High performance FOWLP	Mid performance FOWLP
300mm/HD panel size	200mm panel size
Best solution for mid to large body sizes with >200 I/O	Best solution for smaller body sizes with lower I/O (~100)
Below 10/10 μm line width/line space	Above 10/10 μm line width/line space
Multiple redistribution layers (RDL)	Low profile with overmold structure (100 - 150 μm die thickness)
Heterogeneous integration in 2.5D, 3D, Package-on-Package (PoP) and System-in-Package (SiP)	LGA, BGA and multi-chip packages

Through Silicon Via (TSV)

Through Silicon Via (TSV) utilizes short vertical interconnections or “vias” that pass through a silicon wafer in order to achieve greater space efficiencies and higher interconnect densities than wire bonding and chip chip stacking. When combined with microbump bonding and advanced chip chip technology, TSV technology provides the ability to scale semiconductor devices to smaller and smaller geometries with higher input/output.

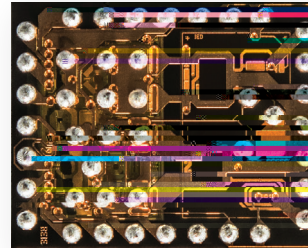
We understand the cost and supply chain limitations our customers face with utilizing TSV technology. The JCET Group is focused on providing customers with cost effective TSV solutions in key areas.

For over two years JCET has been in volume production of 3D TSV for 200mm CMOS Image Sensor (CIS) wafers. The tapered via utilizes a via-last approach to contact the die pad from the wafer backside. This proven approach is also a good fit for other sensor applications such as fingerprint sensors (FPS) or pressure sensors.

For 3D integrated circuits, JCET has a full front- to back-end manufacturing capabilities and currently handles both chip-to-chip (C2C) and chip-to-wafer (C2W) assembly for 3D TSV technology. This includes high density microbump capabilities in both solder and copper column, microbump bonding down to 40 μm pitch, thin wafer handling, wafer-level underfill, thin

wafer dicing and microbumps for chip chip interconnection. Microbump technology is critical to delivering fine pitch, low profile solutions for high performance devices.

Integrated Passive Devices (IPD)



Passive devices such as resistors, capacitors, inductors, filters and baluns can consume 60-70% of available space in a system, subsystem or SiP. As one of the first companies in the industry to integrate and fabricate passive devices at the silicon wafer level, we are able

to produce IPDs which are significantly smaller, thinner and higher performing than standard discrete passive devices that are commercially available today.

With this knowledge and experience, we have embedded passive devices in very close proximity to the active die, providing significant performance, size reduction and device integration in SiP configurations that address 2.5D and 3D integration requirements.